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14. ABSTRACT

New experimental techniques need to be developed to investigate the physical properties of suspended oxide membranes approaching twodimensionality. Here, we report on our progress to demonstrate a robust lithographic patterning method to fabricate self-supported ultra-thin oxides that undergo sharp structural transitions. Utilizing such self-supported membranes, we have directly observed shift in metal-insulator transition temperature arising from stress relaxation and consistent opening of the hysteresis in a model system vanadium dioxide. Electric double layer transistors are then fabricated with the membranes and compared to thin film devices. The ionic liquid allowed reversible modulation of channel resistance and allowed distinguishing bulk process from the surface effects. The techniques developed here can be widley adapted to studies of new materials in 2D suspended form.

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Report Title

Fabrication of suspended oxide membranes and electrical measurements

ABSTRACT

New experimental techniques need to be developed to investigate the physical properties of suspended oxide membranes approaching two-dimensionality. Here, we report on our progress to demonstrate a robust lithographic patterning method to fabricate self-supported ultra-thin oxides that undergo sharp structural transitions. Utilizing such self-supported membranes, we have directly observed shift in metal-insulator transition temperature arising from stress relaxation and consistent opening of the hysteresis in a model system vanadium dioxide. Electric double layer transistors are then fabricated with the membranes and compared to thin film devices. The ionic liquid allowed reversible modulation of channel resistance and allowed distinguishing bulk process from the surface effects. The techniques developed here can be widley adapted to studies of new materials in 2D suspended form.

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(a) Papers published in peer-reviewed journals (N/A for none)

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Number of Presentations: 0.00

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Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

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(d) Manuscripts

Received		Paper
02/14/2014	1.00	J. Sim, Y. Zhou, S. Ramanathan. Suspended sub-50 nm vanadium dioxide membrane transistors: fabricationand ionic liquid gating studies, Nanoscale (07 2012)
02/14/2014	2.00	Maryam Abazari, Masaru Tsuchiya, Shriram Ramanathan, W.-C. Wei. High-Temperature Electrical Conductivity Measurements on Nanostructured Yttria-Doped Ceria Thin Films in Ozone, Journal of the American Ceramic Society (01 2012)
02/14/2014	4.00	Jai S. Sim, B. Viswanath, Shriram Ramanathan, Maryam Abazari. Fabrication and physical properties of thin TixOy membranes from single crystal TiO2, Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films (01 2012)
TOTAL:		**3**

Number of Manuscripts:

Books

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TOTAL:

Patents Submitted

Patents Awarded

Awards

Graduate Students

NAME	PERCENT_SUPPORTED	Discipline
Jai Sim	1.00	
FTE Equivalent:	**1.00**	
Total Number:	**1**	

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
Maryam Abazari	1.00
FTE Equivalent:	**1.00**
Total Number:	**1**

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
S. Ramanathan	0.10	No
FTE Equivalent:	**0.10**	
Total Number:	**1**	

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

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This section only applies to graduating undergraduates supported by this agreement in this reporting period

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Names of Personnel receiving masters degrees

NAME

Total Number:

Names of personnel receiving PHDs

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Names of other research staff

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Inventions (DD882)

Scientific Progress

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Technology Transfer

Project: Fundamental Studies on Confinement Effects in Ionic Conduction Conduction and Inversion Layers in 2-D Single Crystal Free Standing Oxide Membranes
PI: Shriram Ramanathan, Harvard University
Grant: W911NF-10-1-0515

Abstract
New experimental techniques need to be developed to investigate the physical properties of suspended oxide membranes approaching two-dimensionality. Here, we report on our progress to demonstrate a robust lithographic patterning method to fabricate self-supported ultra-thin oxides that undergo sharp structural transitions. Utilizing such self-supported membranes, we have directly observed shift in metal-insulator transition temperature arising from stress relaxation and consistent opening of the hysteresis in a model system vanadium dioxide. Electric double layer transistors are then fabricated with the membranes and compared to thin film devices. The ionic liquid allowed reversible modulation of channel resistance and allowed distinguishing bulk process from the surface effects.

Introduction

Self-supported ultra-thin oxide nanostructures are gaining increased attention due to their potential use in energy and environmental technologies, micro-electromechanical systems, and sensors. For example, structures where functionality is determined by surface to volume ratio (such as but not limited to chemical sensors) could benefit greatly from ultra-thin suspended device architectures. Furthermore, creating such quasi 2-dimensional free standing membrane with correlated oxides may also lead to new insights into mesoscopic electronic phenomena. Vanadium oxide (VO_2) is of contemporary interest as a model material to investigate correlated electron phenomena, metal-insulator phase transition mechanisms, and as well as for potential applications in switching devices. While studies have been conducted on thin films, hybrid layers of VO_2 supported on other materials, and various nanosized and microscale crystals, fundamental phase transition properties and electrical measurements of self-supported VO_2 thin film membranes removed from substrate confinement have not been reported yet to the best of our knowledge, in part due to the experimental challenges in the fabrication of such a structure. In this report, we present fabrication of self-supported edge clamped sub-50 nm vanadium dioxide membrane through an arduous optimization of fabrication processes, and report its electrical properties in Van der Pauw measurements as well as three-terminal field effect device geometry using ionic liquid gate dielectric. Here, we investigate electrolyte gating with ionic liquid on the electrical properties of VO_2 films and membranes and compare the results with annealing VO_2 films and membranes in hydrogen to provide insight into the doping mechanism. The results show that mechanically stable free-standing membrane of VO_2 can be fabricated, could enhance surface effects, and be of potential interest in devices. Further, the techniques presented here are broadly relevant to fabricate self-supported nanostructures for electrical interrogation.

Experimental Details

Nano-scale self-supported free standing membranes have been prepared by the method outlined below. Fig. 1 shows a detailed flow diagram of the processing steps. Double side polished 500um thick Si wafer with 200nm of low stress low pressure chemical vapor deposition (LPCVD) Si_3N_4 on both sides was obtained from University Wafers. Shipley S1813 photoresist

is spun on one side of the wafer and squares with desired sizes are patterned using a Karl-Suss MJB4 mask aligner and CD-26 as a developer. The Si_3N_4 on the patterned areas is etched using a South Bay reactive ion etcher (RIE) to expose the Si substrate. By taking advantage of anisotropic etch of Si in KOH, a membrane of Si_3N_4 on the un-patterned side of the wafer is created. A thin layer of VO_2 is deposited on top of the Si_3N_4 membranes by radio frequency (RF) sputtering from a V_2O_5 target. VO_2 films were grown under different oxygen pressure conditions as a means to tune their electrical properties and experimental conditions are listed in Table 1.

Table 1: Deposition Parameters of Conditions A, B, and C

Sample	Pressure [mTorr]	Power [W]	Ar Flow Rate [sccm]	O_2 Flow Rate [sccm]	Substrate Temperature [˚C]	Thickness [nm]
A	10	150	100	0	550	40
B	10	165	100	0	550	120
C	10	150	100	0.3	450	40

Once the VO_2 film is grown, Shipley S1813 is patterned and used as a mask for etching VO_2 film in unwanted areas, leaving a desired diamond pattern on top of the Si_3N_4 window in such a way that the corners of the diamond pattern are at the midpoint the Si_3N_4 membrane edge. Fig. 2 (a) shows the desired diamond pattern VO_2 on the Si_3N_4 membrane. The selection of a diamond geometry with only the corners touching the substrate is chosen to make Van der Pauw measurements possible. Furthermore, the chosen shape allows the relaxation of stress of the Si_3N_4 during the back side RIE etch. As the low stress LPCVD Si_3N_4 is made thinner, it begins to deform and buckle causing mechanical stress on whatever film is layed on top. Fig. 2(b) shows the buckling pattern of the Si_3N_4 as it is made thinner. From attempting different geometries, it was found that if the VO_2 film had a significant contact with the edge of the Si_3N_4 window, the VO_2 film will crack during the backside RIE of the Si_3N_4 and hence is an important design parameter in fabricating robust membranes. Metal contacts are made at the corners of the diamond pattern by RF sputtering of 6nm Ti and DC sputtering of 200nm of Au for four probe Van der Pauw measurement. Finally, the Si_3N_4 under the VO_2 is etched away from the backside by using RIE leaving a self-supported free standing nano-scale VO_2 membrane as shown in Fig. 2 (d) and (e).

Van der Pauw measurements as a function of temperature were repeated for both VO_2 film on Si_3N_4 and the suspended VO_2 membrane for a comparison of the resistivity (ρ) vs. temperature (T) curves. Afterwards, the VO_2 film on Si_3N_4 (film device), Fig. 2(c), and VO_2 free standing membrane (membrane device), Fig. 2(d), were subjected to systematic ionic liquid gating as well as hydrogen exposure treatments. Ionic liquids are molten salts with high ionic conductivity but negligible electronic conductivity and have been used to modify carrier densities in various semiconducting materials. When applying a gate voltage above its melting temperature, ions can move within the liquid to the ionic liquid/VO_2 interface, forming an electric double layer and inducing carrier density change in VO_2. After cooling below its melting temperature, the mobility of ions in the ionic liquid becomes lower and the ions become frozen at the interface and carrier modulation is preserved even without a gate bias as long as the ambient temperature does not approach the melting temperature. The ionic liquid used in the electrolyte gating experiments is 1,2,3,4,5-pentamethylimidazolium bis(pentafluoroethylsulfonyl)imide (M_5I-Beti) from Covalent Associates Incorporated, USA with a melting temperature of ~ 98ºC.

First, the electrolyte was dropped onto the sample surface at room temperature. Then the temperature was raised to 115 ºC, where the ionic liquid melted and covered the entire surface of VO_2 film/membrane. Gate bias was applied from a probe inserted into ionic liquid while one of the four electrodes was grounded as shown in Fig. 3. The system was kept under a fixed gate bias for 15 minutes at 115 ºC and then cooled down to room temperature with gate bias applied. Afterwards, the gate bias was removed and Van der Pauw measurements were performed with temperature ranging from 20ºC to 90ºC. Another set of both film and membrane devices, (grown at the same time as previous samples,) were fabricated and exposed to 5% H_2 in Ar balance in an environmental probe station for an hour at 100˚C and 150˚C. Then Van der Pauw measurement was performed to obtain ρ vs. T curves and the effect of H_2 on VO_2 film and membrane is compared to that of ionic liquid gating.

Results and Discussion

Fig. 4 (a), (b), and (c) show the temperature dependent resistivity of films and membranes grown under conditions A, B, and C respectively. Fig 4 (d), (e), and (f) show the dlog(ρ)/dT of films and membranes of samples A, B, and C respectively. The transition temperatures were determined by Gaussian peak of the dlog(ρ)/dT curves. One major difference in the electrical properties between a VO_2 film and a free standing membrane grown with no oxygen is that the transition temperature is depressed. In Fig. 4(a) the transition temperature is shifted for the membrane by -6˚C and -8˚C during heating and cooling respectively. In Fig. 4 (b) the transition temperature difference for heating and cooling curves between a film and a membrane ($T_{membrance}$ - T_{film}) are -3˚C and -4.9˚C respectively. A decrease in the VO_2 transition temperature is indicative of manifestation of compressive stress or relaxation of tensile stress. The deformation of the membrane's shape from a square, Fig 2(c), to an asteroid, Fig 2(d), is indicative of relaxation of tensile stress in the membrane, which is in agreement with the shift in the transition temperature going from a film to a membrane in our devices. In condition C, the deposition parameters were optimized (through background oxygen partial pressure tuning achieved by oxygen flow control) to yield a nearly stress-free VO_2 film on Si_3N_4. The correlation between oxygen partial pressure during the deposition and the oxygen content in the film has been studied previously by X-ray photoelectron spectroscopy[13] and was used to optimize the growth condition. This is evident in fig. 4(c) where the transition temperature during heating is close to that of bulk single crystal VO_2 (~ 68 ºC) for both films and membranes. In addition, the transition temperature does not shift much between the film and membrane. Also from fig. 4(c) the activation energy is found to be 0.191eV and 0.196eV for the insulating state and 0.098eV and 0.103eV for the metallic state of the film and the membrane respectively, showing that the conduction mechanism does not change between the film and membrane. There is observable hysteresis widening after making membranes from the stress-free films. Fig. 4 (f) shows the hysteresis width changing from 7˚C to 11˚C for the film grown with condition C. Fig. 4 (d), (e), and (f) all show an increase in the width of the hysteresis regardless of the deposition conditions. In fig. 4 (d) the hysteresis opens up from 14˚C to 16˚C and in fig. 4 (e) the hysteresis opens up from 5.5˚C to 7.4˚C. The opening of the hysteresis can be explained by amplified surface effect in a self-supported membrane. Fig. 5 shows the log(ρ) vs. T for film and membrane devices at various bias voltages in electrolyte gating experiments. At gate bias of 2V the resistivity of the insulating state at 25 ºC of the film and the membrane are 0.97Ω-cm and 0.761Ω-cm respectively, showing a slight decrease from the original insulating state resistance. At a gate bias of 2.5V the resistivity of the film and the membrane are further reduced to 0.12Ω-cm and

0.067Ω-cm respectively. There is a clear trend that the resistivity of the membranes is much lower than that of the film, which is clearly evident in fig. 5. This could be explained by carrier doping near the ionic liquid-VO_2 interfaces. Thus, having two exposed surfaces in the membrane naturally increases its response. This is demonstrated extremely well when the film and the membrane are gated at 2.5V in that the resistivity of the insulating state of the membrane is only ~56% of the insulating state of the film. The doping from the ionic liquid is not a permanent chemical change but a reversible process. Hydrogen annealing studies were conducted on the film and membrane devices to compare the results to the ionic liquid gating results to better understand the doping mechanism. The change in the resistivity of the insulating phase is about 22% for the film and 21% for the membrane for hydrogen exposure at 100°C. The membrane does not seem to be more sensitive to the H_2 than the film at this temperature. For 150˚C exposure, the resistivity change is about 64% for the film and 70% for the membrane, again not a large difference between the film and the membrane unlike observed in ionic liquid gating. The lack of a large difference in change of resistivity of the insulating state in H_2 between the film and the membrane is likely due to the rapid diffusion of H_2 throughout thickness of VO_2. The transition temperature of the film during heating decreases slightly from 68.0 ºC to 67.0 ºC at 2V gate bias and 64.3 ºC at 2.5V. On the other hand, the transition temperature of the membrane changes from 67.3 ºC to 66.0 ºC at 2 V gate bias and is further reduced to 62.1 ºC at 2.5 V gate bias. Utilizing experimentally determined relationships between transition temperature of doped vanadium dioxide and carrier density one can estimate the accumulated carrier density from the change in the metal-insulator transition temperature. In general, chemically reducing V^{4+} into V^{3+} and therefore doping VO_2 with electrons could destabilize insulating M1 phase with respect to metallic rutile phase and decrease the transition temperature. In compounds such as $V_{1-X}M_XO_2$ (M = Mo, W), the metal-insulator transition temperature changes with the chemical doping as $dT_{MI}/dx \sim -2300\sim2570$K/ atomic %.[19] Based on this relation, we can extrapolate the electron doping density for the membranes. If 0.2 % electron doping per vanadium atom is roughly assumed, which corresponds to $\sim 1 * 10^{20}$ cm^{-3} bulk carrier density change, it could lead to decrease in transition temperature of ~5 K. Using this value, the accumulated sheet carrier density for a 40 nm thickness membrane is $4*10^{14}$ cm^{-2}. From this value we can estimate the effective capacitance of the ionic liquid could be estimated as ~ 60 $\mu F/cm^2$ in the free-standing membrane device geometry.

Summary

We have developed a robust fabrication process for self-supported edge clamped oxide membranes that are stable under rigorous electrical characterization. The fabrication process can be adapted to a range of nano-scale materials systems that require electrical characterization. Utilizing such suspended membranes, we have directly observed shift in metal-insulator transition temperature likely arising from stress relaxation and opening of the hysteresis. Ionic liquid gating of the membrane transistors allowed reversible modulation of channel resistance. The technique is being developed presently to extend to ionic-electronic conducting oxides that undergo large lattice distortions and hence require extraordinary care in fabricating robust structures.

Selected references

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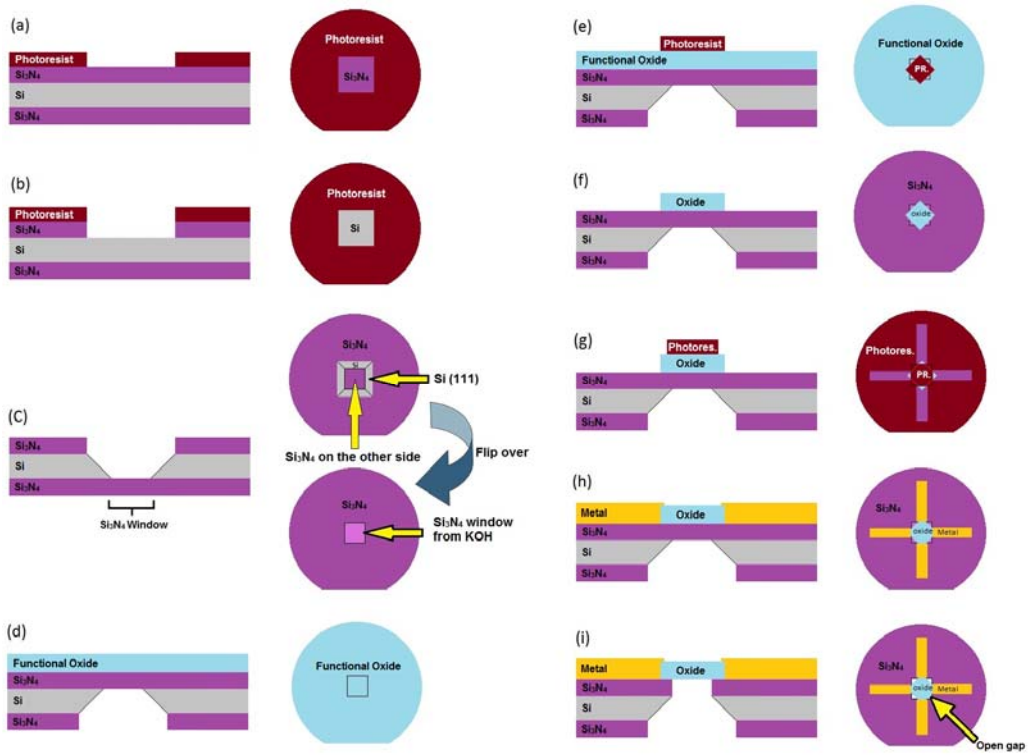

Figure 1: Process diagram of the ultra-thin membrane fabrication process
(a) S1813 is spun on the wafer and patterned, (b) The Si_3N_4 in the patterned area is etched using RIE (c) The Si substrate is etched using KOH, leaving behind a small Si_3N_4 membrane on the unpatterened side, (d) Functional Oxide (in this VO_2) is deposited on the unpatterned side of the wafer, (e) S1813 is spun on and patterened leaving a diamond patterned resist over the Si_3N_4 membrane, (f) The oxide in the unwanted area is etched away using RIE, (g) S1813 is spun on and patterned for metal contacts at the corners of the oxide, (h) Desired metal (Ti/Au) is deposited and lifted off to create metal contacts, (i) The Si_3N_4 under the oxide is etched away by RIE from the back side of the wafer.

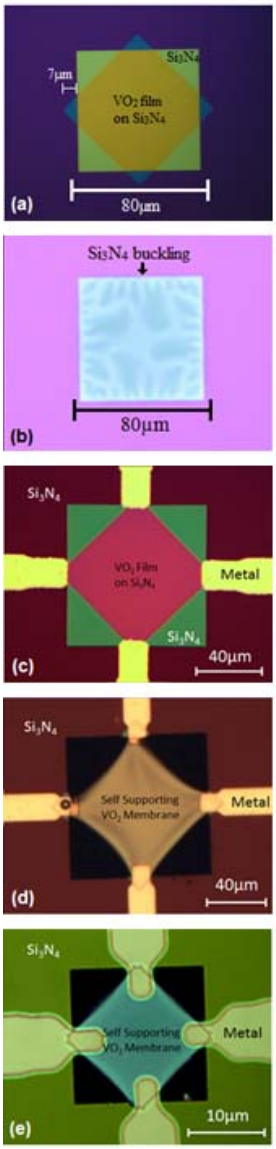

Figure 2: Optical Images of Si_3N_4 Membrane and VO_2 Film and Membrane Devices. (a) VO_2 film patterned into a diamond, (b) Si_3N_4 membrane buckling (c) 80um diagonal VO_2 film on Si_3N_4, (d) 80um diagonal free standing VO_2 membrane, (e) 20uμm diagonal free standing VO_2 membrane. The images are in false color. (a) Note how only the corners of the oxide touch the edge of the Si_3N_4 Membrane. This is a crucial step for the oxide to be robust during RIE. (b) The purple area is Si_3N_4 on Si and the blue area is Si_3N_4 membrane. Note that there is large distortion from Si_3N_4 buckling due to low stress Si_3N_4 being clamped to the Si at the edge of the membrane. The buckling occurs during RIE as the thickness of Si_3N_4 membrane is reduced. Any oxide present near the edge of the Si_3N_4 membrane results in cracking during RIE due to this buckling. Hence, our geometry was chosen from numerous experiments to minimize contact with the edge of the Si_3N_4 membrane. The black spaces in (c) and (d) are free space. Note that the distorted shape of the VO_2 membrane in (d) is from relaxation of tensile stress. (e) the device in this figure has minimal distortion.

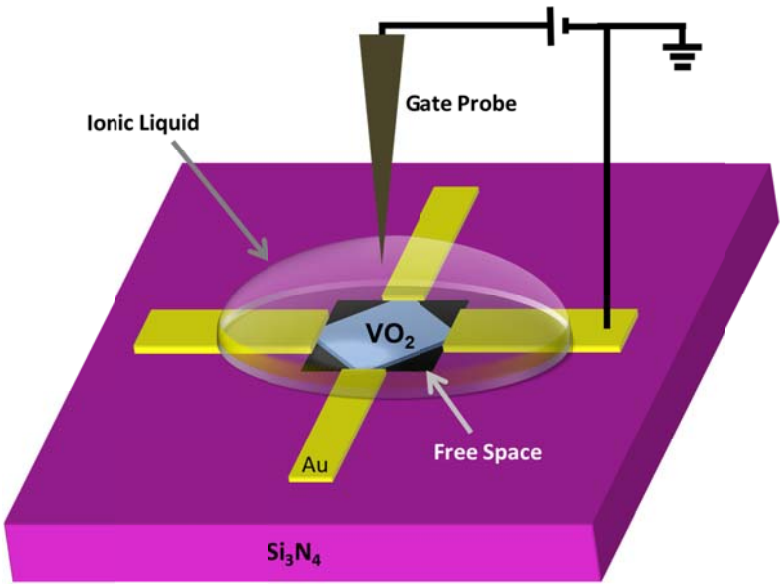

Figure 3: Schematic of Electrolyte Gating of VO_2 forming an electric double layer transistor. The VO_2 membrane is completely submerged in the ionic liquid.

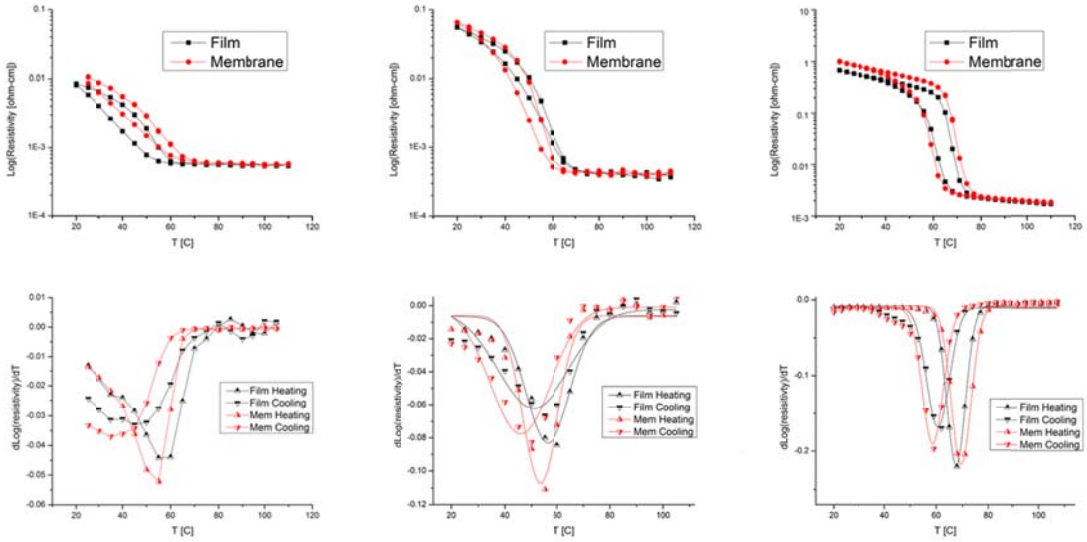

Figure 4: (a), (b), (c) Temperature vs. Resistivity ρ plots, (d), (e), (f) Temperature vs. Derivative of the Log(ρ). Note that for (a) and (b), the transition temperature is depressed due to the relaxation of tensile stress. The tensile stress originates from lack of O_2 during deposition. In (c) the O_2 partial pressure is optimized during deposition to yield a nearly stress-free VO_2 and the transition temperature is comparable to that of bulk single crystals. One trend that is consistent in all of the samples was that the width of the hysteresis increased. Gaussian fitting did not yield a good fit for (d).

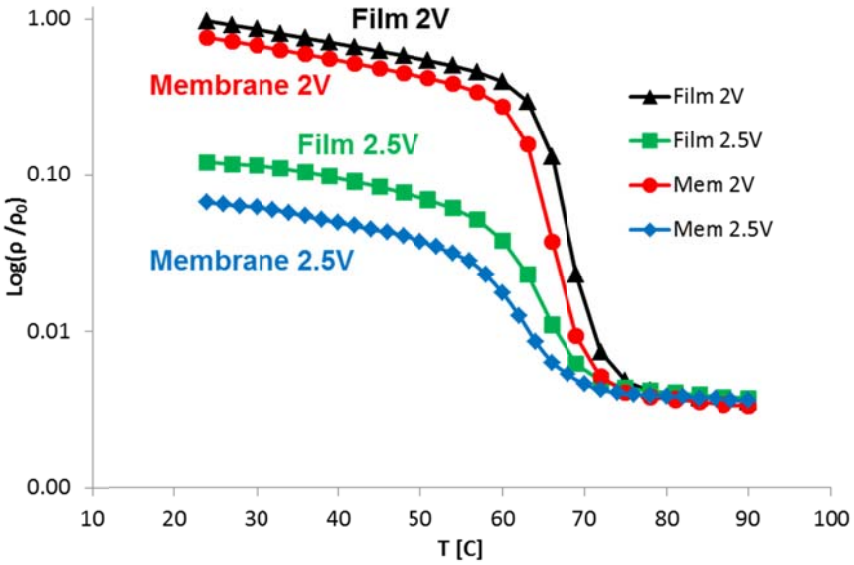

Figure 5: Temperature vs. Resistivity ρ Plot of VO_2 Devices with Various Ionic Liquid Gate Voltages. At gate bias of 2V the resistivity of the insulating state at 25 ºC of the film and the membrane are 0.97Ω-cm and 0.761Ω-cm respectively. At a gate bias of 2.5V the resistivity of the film and the membrane are further reduced to 0.12Ω-cm and 0.067Ω-cm respectively. Note that the membrane is consistently more sensitive to the ionic liquid gating from the increased surface coverage.